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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/914,928	09/06/2001	Loick Verger	034299-346	5963

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EXAMINER	
SUNG, CHRISTINE	
ART UNIT	**PAPER NUMBER**
2878	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/914,928	VERGER ET AL.	
	Examiner	Art Unit	
	Christine Sung	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. The amendment filed on April 18, 2005 has been entered.

2. The Request for Continued Examination file on April 18, 2005 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 7-9, 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeromin (US Patent 5,381,014 A) in view of Patch (US Patent 6,126,901 A).

Regarding claim 1, Jeromin discloses and x-ray imagery device (figure 1) comprising at least one detection matrix made of a semiconducting material (elements 14,15 and 19), said detection matrix comprising:

Pixels (elements 17) to convert incident x-photons into electric charges (Column 3, line 1);

An electric charges reading panel (element 15) including a plurality of electronic devices (element 19), each electronic device be integrated by pixel (elements 17 and 19);

A detection layer (element 14) made of a continuous layer of semiconducting material deposited in vapor phase (column 3, lines 27-30) on the electric charges reading panel (see figure 1). Jeromin does not specify that the electric charges reading panel is made of monocrystalline silicon. However, Patch discloses a conventional single crystalline silicon substrate or electric charges reading panel (column 8, lines 57-60). One of ordinary skill in the art would be

motivated to use the substrate or electric charges reading panel as disclosed by Patch with the invention as disclosed by Jeromin in order to increase detection efficiency.

Regarding claim 2, Jeromin discloses a process for making an x-ray image device (figure 1) comprising at least one detection matrix made of a semiconducting material (elements 14, 15 and 19), said detection matrix comprising pixels (element 17) to convert incident x-photons into electric charges (column 3, line 1) and an electric charges reading panel (element 15) including a plurality of electronic devices (element 19), each electronic device being integrated by pixel (elements 17 and 19), wherein each detection matrix is obtained by vapor phase deposition of a semiconductor on the electric charges reading panel (column 3, lines 27-30) on the electric reading panel (see figure 1). Jeromin does not specify that the electric charges reading panel is made of monocrystalline silicon. However, Patch discloses a conventional single crystalline silicon substrate or electric charges reading panel (column 8, lines 57-60). One of ordinary skill in the art would be motivated to use the substrate or electric charges reading panel as disclosed by Patch with the invention as disclosed by Jeromin in order to increase detection efficiency.

Regarding claim 3, although Jeromin in view of Patch does not explicitly state that the specific temperature of the deposition process of the semiconducting material be at a temperature that does not damage the electronic devices, it would have been obvious to one having ordinary skill in the art to have chosen a semiconducting material whose vaporization temperature would not exceed the highest tolerable temperature of the electronic devices, so as to not render the device useless.

Regarding claim 4, Jeromin discloses that the semiconducting material is made of mercuric iodide (Column 3, lines 47-48).

Regarding claim 7, Jeromin discloses that the detection layer (element 14) is deposited directly on the electronic devices (element 19) of the electric charges reading panel (element 15) in each pixel.

Regarding claim 8, Jeromin discloses that the detection layer is made of semiconducting material (see abovementioned paragraphs), but does not specify crystalline silicon. However, although Jeromin does not specify that crystalline silicon is used, he does disclose that crystalline is a well known semiconductor (column 5, lines 49-53), and further teaches that the specific type of radiation detecting material selected will depend upon the desired charge generation efficiency. One of ordinary skill in the art would be motivated to use crystalline silicon as the detection layer because it has excellent detection efficiency, which would increase the accuracy of the detected data.

Regarding claim 9, Jeromin discloses that element 19, is a transistor-capacitor element, which inherently contains an amplifier, a preamplifier and filter. Further, Jeromin discloses that the detector has an image processor (Column 7, lines 23-39).

Regarding claim 11, Jeromin discloses a method for making an x-ray image device (figure 1) comprising at least one detection matrix made of a semiconducting material (elements 14, 15 and 19), said detection matrix comprising pixels (element 17) to convert incident x-photons into electric charges (column 3, line 1) and an electric charges reading panel (element 15) including a plurality of electronic devices (element 19), each electronic device being integrated by pixel (elements 17 and 19), said method comprising:

Forming the electronic devices (element 19) on a substrate (element 13) to produce the electric charges reading panel (element 15) of each detection matrix; and

vapor phase depositing a semiconductor on the electric charges reading panel (column 3, lines 27-30) on the electric reading panel (see figure 1) so as to form a detection layer (element 14) made of a continuous layer of the semiconducting material.

Jeromin does not specify that the electric charges reading panel is made of monocrystalline silicon. However, Patch discloses a conventional single crystalline silicon substrate or electric charges reading panel (column 8, lines 57-60). One of ordinary skill in the art would be motivated to use the substrate or electric charges reading panel as disclosed by Patch with the invention as disclosed by Jeromin in order to increase detection efficiency.

Regarding claim 12, although Jeromin in view of Patch does not explicitly state that the specific temperature of the deposition process of the semiconducting material be at a temperature that does not damage the electronic devices, it would have been obvious to one having ordinary skill in the art to have chosen a semiconducting material whose vaporization temperature would not exceed the highest tolerable temperature of the electronic devices, so as to not render the device useless.

Regarding claim 13, Jeromin discloses assembling more than one detection matrix to form a large area digital detector (see figure 4).

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeromin (US Patent 5,381,014 A) in view of Patch (US Patent 6,126,901 A) further in view of the admitted prior art.

Regarding claims 5-6, Jeromin in view of Patch does not specify that the electronic devices are made using a process technology having feature device sizes of 0.1 micron or 1.25 microns. However, on page 7, lines 26-30 of the specification, applicant acknowledges that the

feature sizes are conventional. One of ordinary skill in the art would be motivated to use the conventional feature device sizes in order to reduce costs and use conventional semiconductor device processing methods instead of developing non-conventional methods which are costlier.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeromin (US Patent 5,381,014 A) in view of Patch (US Patent 6,126,901 A) further in view of Mori et al (US Patent 4,591,984 A).

Regarding claim 10, Jeromin in view of Patch discloses the limitation set forth in claim 9, but does not specify the conventional processing circuit with a reading circuit and integration circuit and a counting circuit. Conventional processing techniques use such circuits in order to properly process the collected data, as demonstrated by Mori (see Figure 3, and column 2, line 59-column 3, line 3). On of ordinary skill in the art would be motivated to use the claimed circuits in order to properly process the detected image signals and to reduce errors.

Response to Arguments

7. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Sung whose telephone number is 571-272-2448. The examiner can normally be reached on Monday- Friday 7-3 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on 571-272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine Sung
Examiner
Art Unit 2878

CS